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A Novel Five-Level Inverter Configuration for PV Systems

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Abstract: In this paper, a fault-tolerant single-phase five-level inverter configuration is proposed for photovoltaic (PV) generation systems. Conventional two-level inverters are popularly used in PV applications, but these inverters provide the output voltage with considerable harmonic content. One of the efficient ways to improve the power quality of PV generation systems is to replace a two-level inverter with a multilevel inverter. Conventional multilevel inverters reduce total harmonic distortion and filter requirements effectively, but it has limitations in terms of reliability due to increased device count and capacitor voltage balancing issues. Therefore, a fault-tolerant single phase five-level inverter is presented, which is constructed by using a half-bridge two-level inverter, a three-level diode clamp inverter, and a bidirectional switch. The proposed inverter topology can tolerate the system faults due to failure of the source and/or switching devices with least modification in the switching combinations. It has less number of switching devices compared to conventional five-level inverters. The topology also has the energy-balancing capability between sources which helps in reducing uneven charge of batteries in case of partial shading or hotspots on one side of the PV panels. The proposed system under normal and faulty condition is simulated in MATLAB/Simulink environment, and results are verified with a laboratory prototype.

Index Terms: Fault-tolerant multilevel inverters, photovoltaic (PV) generation system, power quality, total harmonic distortion (THD).

I. INTRODUCTION

Renewable-Energy sources such as solar and wind energy systems are gaining more attention both in research and industry communities to reduce the dependence on conventional fossil fuel systems [1]. In particular, the continuous improvement in semiconductor technology for solar cell fabrication increases the cell efficiency and hence motivates the use of photovoltaic (PV) systems widely [2]. In order to drive the ac loads, the PV generation system uses a two stage conversion process which involves boosting up the low array voltage, followed by inversion [3], [4]. To minimize the losses involved in each stage, this two-stage conversion process is reduced to single stage using boost inverters [5], [6]. The single-stage conversion improves the efficiency by reducing losses but suffers from disadvantages such as poor harmonic profile of the output voltage and higher filter requirement due to the use of a two-level inverter. Conventional multilevel inverters are introduced in [7] and [8], which reduce filter size requirement and improve power quality of PV generation systems by reducing total harmonic distortion. However, these multilevel inverters offer limitations in terms of more number of power device requirement for a given number of voltage levels [9], capacitor voltage balancing problems, and reliability issues. By addressing some of the aforementioned issues, many multilevel inverter topologies are presented in literature with reduced number of devices for PV generation systems and drive applications [10]–[14]. In these topologies, although the switch count is reduced, any one of the switch or source failure may lead to overall system shutdown.

The off-grid PV generation system is a preferable choice for electrification option for geographically remote areas and islands which are far from the grid [15]. The faults in these systems such as source and switch failure may cause overall system shutdown and take longer time to recover. These issues bring in the need of fault-tolerant converters for PV generation systems to provide continuous power to essential loads. In this regard, switch failure issues of multilevel inverters are addressed in [16] without compromising on the number of levels even under fault condition. In [17], a fault-tolerant topology for grid connected PV application using a coupled Scott transformer is proposed. In normal condition, the topology operates with less number of switches, but during fault, it requires an additional leg to replace the faulty switch. The survey of fault-tolerant techniques for three-phase two-level and multilevel inverters is discussed in [18] and [19]. Also, it has clearly discussed the importance and need for continuous development of fault tolerant multilevel inverters. The paper given in [20] presents an open-circuit fault-tolerant control strategy for a T-type three level inverter without using additional switches. The previously discussed topologies [16]–[20] with single or multiple sources have no fault tolerance capability with respect to source failure and energy-sharing capability.

To address the previously discussed issues in this paper, a single-phase five-level inverter topology is proposed for PV applications. The proposed topology has fault-tolerant capability in case of any one of the source and/or switch open fault. The accomplishment of fault tolerance with least changes in switching pattern and less number of

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active switches makes the topology more reliable. The proposed topology also has the major advantage of energy-balancing capability between sources to minimize the difference in state of charge of batteries (SOC). The unbalance in SOC of batteries may be because of partial shading or hotspots on any one side of the PV string.

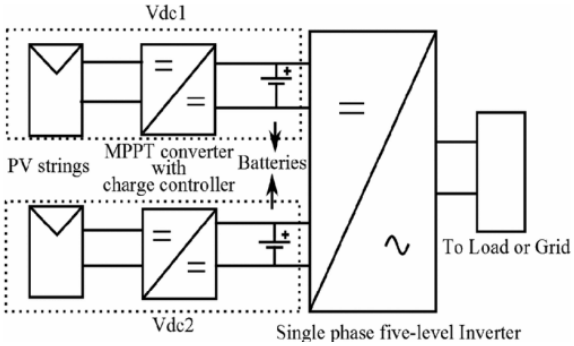

Fig 1. Block diagram of the single-phase five-level inverter.

The rest of this paper is organized as follows. The description and operation of the topology along with adapted pulse width Modulation (PWM) is explained in Section II, the results are described in Section III, and the performance of the system is summarized at the conclusion.

II. PROPOSED SYSTEM DESCRIPTION AND OPERATION

The block diagram of the proposed fault-tolerant single phase five-level inverter circuit is shown in Fig. 1. The configuration consists of two separate PV strings, an MPPT converter with charge controller, and associated batteries forming two dc links for the proposed five-level inverter, which are rated at half of the total power rating. The PV array consists of modules which has series- and parallel-connected cells and is modeled using (1) [21]. The maximum power is tracked using the perturb and observe algorithm given in [22].

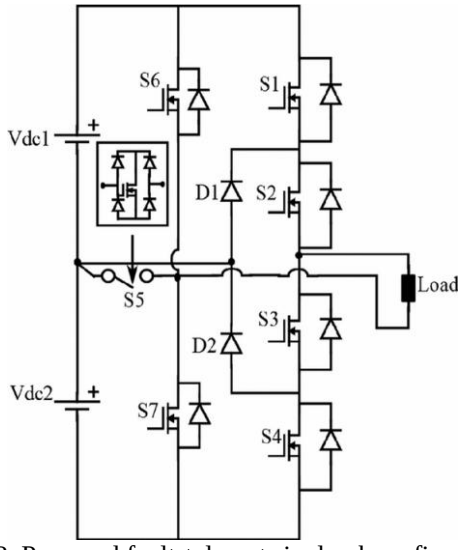

Fig. 2. Proposed fault-tolerant single-phase five-level inverter.

For better understanding, the topology is supplied by two equal dc links Vdc1 and Vdc2, respectively. It is known that a leg of a three-level inverter is capable of generating voltage levels of Vdc1, 0, and −Vdc2; similarly, the two-level half-bridge inverter can generate two voltage levels with magnitudes of Vdc1 and −Vdc2. As a result in combining both, the total effective voltage across the load will have a total of five voltage levels with magnitudes of +(Vdc1 + Vdc2), Vdc1, 0, −Vdc2,and −(Vdc1 + Vdc2). If two dc links are balanced to be of equal magnitude Vdc1 = Vdc2 = 0.5Vdc, then it will generate five voltage levels +Vdc, +0.5Vdc, 0, −0.5Vdc, and −Vdc like the conventional multilevel inverter.

TABLE I SWITCHING COMBINATION FOR FIVE-LEVEL OPERATION

Voltage levels	S1	S2	S3	S4	S5	S6	S7
V_1	1	1	0	0	0	0	1
V_3	0	1	1	0	1	0	0
V_5	0	0	1	1	0	1	0
GROUP I supplied by source Vdc1							
V_2	1	1	0	0	1	0	0
V_4	0	1	1	0	0	1	0
GROUP II supplied by source Vdc2							
V_2	0	1	1	0	0	0	1
V_4	0	0	1	1	1	0	0

The switching combination for five-level voltage generation and direction of current during each voltage level is given in Table I and illustrated in Fig. 3(a)–(j). The switch S5 provides switching redundancy for voltage levels 0.5Vdc, 0, and −0.5Vdc which can help in the energy sharing between two sources due to partial shading on one side of the PV panels. The switching combination for energy balancing between sources in case of partial shading is given in Table II. The additional advantage of bidirectional switch S5 is to continue the operation of the inverter as three levels in case of switch or source failure, which is discussed in detail at the later part of this section. From the proposed converter, it can be observed that the maximum voltage rating of the switching devices S1–S5 is 0.5Vdc, and for S6 and S7, it is Vdc. In Table I, if SA = 1 switch is on, SA = 0 switch is off, where A = 1, 2, . . . , 7.

A. Energy Sharing Between Sources Due to Partial Shading

The mismatch of power generation in PV systems may be because of partial shading, hotspots, etc. Partial shading occurs due to shadow of clouds, trees, and shadow of one panel on the other panel. This causes reduction in power and leads to uneven charging/discharging of associated batteries that results in unequal SOC. Generally, in any island PV generation system, the load has to supply more time from battery power compared to solar power [23]. If the batteries continue to operate with uneven SOCs, the battery with low SOC dries out faster and causes overall system shutdown which, in turn, leads to underutilization of the other battery. The SOC of batteries is calculated

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based on voltage level [24].

An effective energy-balancing technique to balance the charging/discharging of batteries in case of uneven SOCs is derived using the redundant switching states of middle voltage levels of the proposed converter. During a higher voltage level ($+V_{dc}$ and $-V_{dc}$), both sources are connected in series to generate the required voltage level, which can be noticed from Fig. 3(a) and (i).

For better understanding, only positive half-cycle voltage waveforms are shown in Fig. 4(a) and (b). Because of half-wave symmetry, the calculations are done for only the half cycle of the fundamental waveform. The voltage waveforms from 0 to θ and (π − θ) to π correspond to the middle voltage level (V_2) and zero voltage level (V_3). The voltage waveform from θ to (π − θ) is a combination of the higher ($V_1 = V_{dc}$) and middle ($V_2 = V_{dc}/2$) voltage levels. In Fig. 4(a), from θ to (π − θ), the amount of area corresponding to each pulse of the higher level (V_{dc}) pulsating voltage waveform has the same area below the $V_2(V_{dc}/2)$ voltage level also. Hence, Fig. 4(b) represents area A1 corresponding to V_{dc} voltage level and area A2 corresponding to $V_{dc}/2$ voltage level.From Fig. 4(b), the instantaneous voltage from 0 to π given as

$$V = Vm \sin(\omega t)$$

B. Fault Analysis of the Five-Level Inverter

TABLE III SWITCHING COMBINATION TO GENERATE THREE-LEVEL VOLTAGE DURING FAULT

Case-I Vdc2 Source open or short circuit fault and/or S4 or/and S7 Switch Open fault							
Voltage levels	S1	S2	S3	S4	S5	S6	S7
$+0.5V_{dc}$	1	1	0	0	1	0	0
0	0	1	1	0	1	0	0
$0.5V_{dc}$	0	1	1	0	0	1	0
Case-II Vdc1 Source open or short circuit fault And/or S1 or/and S6 Switch Open fault							
$+0.5V_{dc}$	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0
$-0.5V_{dc}$	0	0	1	1	1	0	0

Generally, inverter failures are mainly due to semiconductor switch, source, and driver circuit failures [20]. In the proposed five-level inverter, fault tolerance is done by considering any one of the source short- or open-circuit fault and/or switch open-circuit fault (S1, S4, S6, and S7). In this topology, middle switching device (S2 and S3) failure is also possible by replac-ing clamping diodes D1 and D2 with two extra switches. The possible switching combination for failure of the source and/or switch is given in Table III.

In case of failure (source or switch), only one source will be active, and the total power supplied by the source is half at half of the rated voltage; therefore, to avoid the overloading on the inverter, load management is suggested. During fault, the topology will be operated as a three-level inverter, and the output voltage is maintained at rated value by using the center tap transformer at the load side as shown in Fig. 6.

When the modulating signal (sine wave; Vm) is compared with the upper triangular wave (Vm > Vcr1) and lower trian-gular wave (Vm < Vcr4), higher voltage levels ($V_{dc} - V_{dc}$) are generated using switching Table I. If the modulating sig-nal compares with middle triangles (Vm > Vcr2, Vm < Vcr3), middle voltage levels ($0.5V_{dc}$, $-0.5V_{dc}$) are generated, which has redundancy in switching selection using Tables I and II ex-plained in the flowchart. A zero voltage level is generated using the minimum switching combination given in Table I. In case of fault, the modulating wave will become half and compare with two inner carriers (Vcr2 and Vcr3) The corresponding three-level voltages are generated using Table III.

The number of components for the proposed topology is compared with the five-level neutral-point-clamped, flying capacitor, and H-bridge multilevel inverters, and the topology presented in [16] as shown in Table IV. From Table IV, it is clear that the proposed topology requires less number of switches and clamping diodes than conventional topologies.

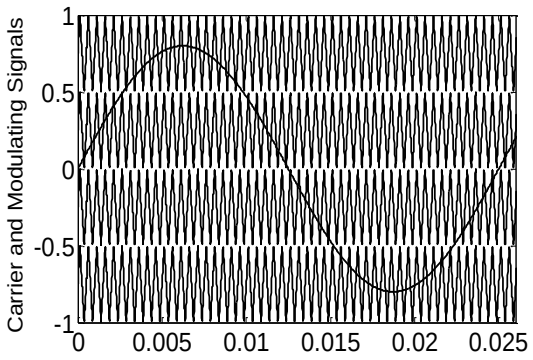

Fig. 4: Modulating and carrier waves for generating pulses in SPWM.

TABLE IV NUMBER OF COMPONENTS FOR THE SINGLE-PHASE FIVE-LEVEL INVERTE

Type of Components	Number of components required				
	In Conventional Topologies			Topology Proposed in [16]	In Proposed topology
	NPC	Flying capacitor	H-bridge		
Main switches	8	8	8	22	7
Main diodes	8	8	8	22	10
Clamping diodes	12	0	0	0	2
DC bus capacitors/ Isolated supplies	4	4	2	1	2
Flying capacitors	0	6	0	7	0
Reliability during switch	No	No	Yes	Yes	Yes
Reliability during Source failure	No	No	Yes	No	Yes

III. SIMULATION RESULTSAND DISCUSSION

The five-level output voltage waveforms across the load and current through the load are shown in Fig. 5 for a

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modulation index of 0.9. Fig. 6 clearly shows five voltage levels and nearly sinusoidal load current waveform. In Fig. 7, after 0.1 s, the fault is created, and the voltage transition from five levels to three level is shown and also demonstrates that the voltage and current magnitudes are reduced.

The rated output voltage of the inverter is maintained by using a primary center tap single-phase transformer, and the corresponding waveforms are observed in Fig. 7. From Fig. 7, after 0.1 s, the fault is created, and the conversion of the voltage waveform from five level to three level with the same magnitude can be observed. From Fig. 7, it can be observed that the magnitude of the current waveform is reduced by suggesting proper load management to avoid overloading on the inverter. At the time of fault, the primary turns of the transformer become half by using the combination of S8 and S9 relays and maintain the volt/turn ratio constant, which results to rated voltage at the secondary side of the transformer.

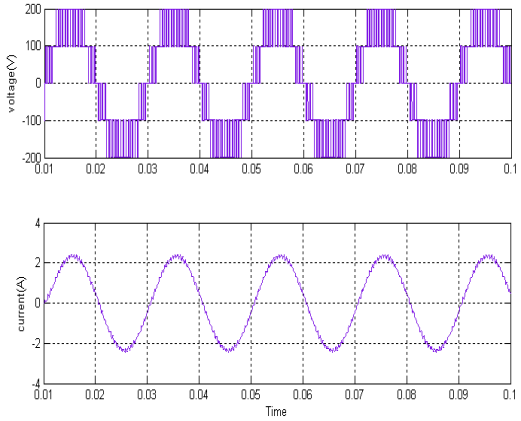


Fig. 5. Output voltage (upper trace) and current (bottom trace) waveforms of the five-level inverter (Y -axis 200 V/div, 2 A/div; X-axis10 ms/div).

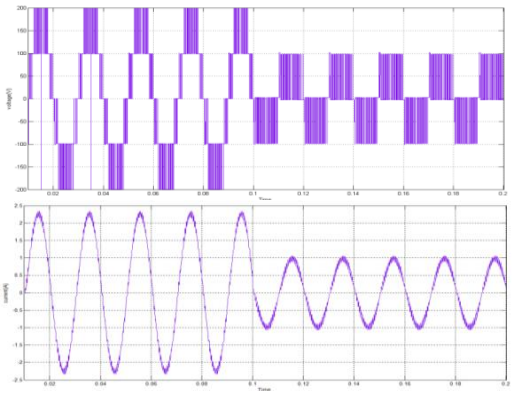
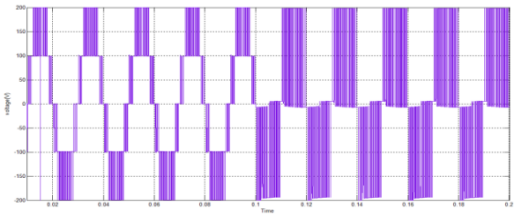


Fig. 6. Output voltage and current waveforms of the proposed inverter due to Vdc2 source failure (Y -axis 200 V/div, 2 A/div; X-axis 20 ms/div)



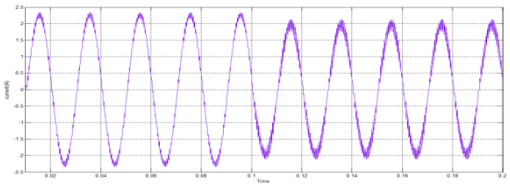


Fig. 7. Output voltage and current waveforms with a transformer due to Vdc2 source failure (Y -axis 200 V/div, 2 A/div; X-axis 20 ms/div).

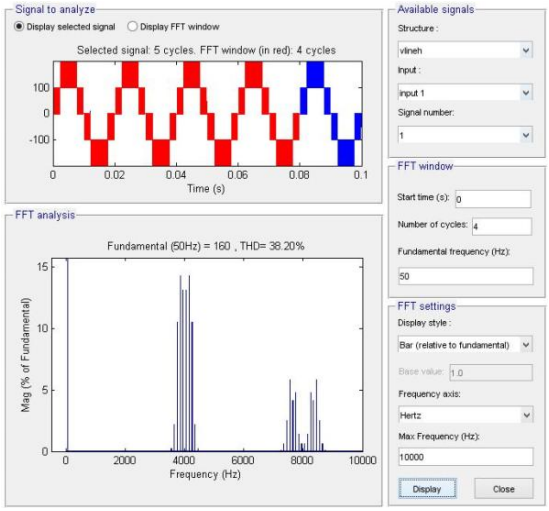


Fig. 8: Harmonic spectrum for phase voltage.

From fig.8, it can be observed that there are no harmonics appearing in between 0 and 3500Hz. Therefore by using this PWM technique harmonic profile can be improved.

IV. CONCLUSION

In this paper, a fault-tolerant single-phase five-level inverter has been presented for PV applications. The proposed topology is simulated, and then The five-level output voltage is achieved by using one leg of a three-level neutral point inverter and a two-level half-bridge inverter. Phase disposition carrier based PWM is adapted in generating the five-level output voltage. The energy balancing between sources is achieved using redundant switching combination at the time of uneven charging of batteries due to partial shadow or hotspots on one side of the PV string. In case of any one of the source and/or switch fails, the topology can be operated as a three-level inverter with the help of a bidirectional switch, and the magnitude of the output voltage is reduced to half. The rated voltage is maintained during fault condition with the help of a transformer. In this configuration, the capacitor voltage balancing issue is minimized and also requires less number of active switches compared to conventional NPC and flying capacitor five-level inverters.

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